PLDshell Plus Design Software

- Easy-to-Use Design Environment for Programmable Logic Design Using Intel μPLDs and the FLEXlogic Family of FPGAs
- Compiles PALASM* 2-Compatible Source Files into JEDEC Programming Files
- Functionally Simulates Designs Using Source File Simulation Syntax
- Easy-to-Learn Menu Interface with Extensive Help and On-Line Technical Support Information
- Editor and Programming Software Configurable to Designer's Preferred Tools
- Merges Multiple PDS Files into Single Device
- Estimates Design Fit Quickly to Narrow Target Device Choices
- Run Menu Configurable to Allow Use with Designer's Existing PLD Design Tools
- Utilities Disassemble/Convert Common PAL/GAL JEDEC Files into Source or JEDEC Files for Intel μPLDs
- Translates ADF/SMF Files into PDS Source Files
- Includes APT Programming Software for Use with Intel Programmers
- Software and Programming Hardware Available through Intel Authorized Sales Office/Distributor
- Standalone Software (No Programming Hardware) Available Free from Intel Literature

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INTRODUCTION

PLDshell Plus design software provides an easy-to-use menu system for programmable logic design that allows you to invoke Intel's PLDasm compiler/simulation software and APT programming software, or your existing programmable logic compilers and programming software. Configure the menu system with the program and directory names of your existing programmable logic design tools and you are ready to run.

PLDshell Plus software includes Intel's PLDasm logic compiler/simulator software. PLDasm software compiles PALASM* 2-compatible source files to produce JEDEC files for Intel μPLDs (Microcomputer Programmable Logic Devices) and FLEXlogic family of FPGAs. Simulation syntax supports functional simulation and generation of test vectors for the JEDEC file. PLDasm software allows you to use a familiar design language to evaluate the architecture of Intel μPLDs and FPGAs and to implement new designs.

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*GAL is a registered trademark of Lattice Semiconductor, Inc.

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PLDshell Plus OVERVIEW

The PLDshell Plus Main Menu is arranged to follow the typical PLD design flow: Edit, Compile/Simulate, View, and Program. PLDshell Plus menu options allow you to:

Edit—Edit PLD source files (or any other text file) using your preferred ASCII text editor. You can configure the edit menu to invoke whatever text editor you have installed in your system via the **Change Editor** button.

Compile/Sim—Compile and/or simulate PLDasm source files to create JEDEC files for Intel μPLDs using Intel's PLDasm software. You can define compile/simulate options such as logic minimization, DeMorgan's inversion, pin assignment algorithm options, and event threshold for asynchronous events (during simulation).

View—View source, error, report, or simulation files to validate your design or quickly locate design or fitting problems. When viewing an error file, you can display on-line error message help information. Simulation results can be viewed in table or wave form. (Waveforms can be viewed on Hercules, EGA, or VGA monitors.)

Program—Invoke Intel's APT programming software. You can change the program menu to your preferred programming software via the **Change Programming S/W** button.

Run—Run up to 24 user-defined programs including other PLD development tools. The menu is user-defined, with each menu option including default command line options and working directories. You can also run any program via the **Run Other** submenu.

Utilities—Provides several utility functions, including:

Disassemble, allows you to disassemble JEDEC files for common PAL/GAL devices into PLDasm source files for Intel μPLDs (JEDEC file to PDS file).

Convert, performs a full conversion (common PAL/GAL JEDEC file to Intel μPLD JEDEC file).

Translate, translates ADF/SMF files developed for Intel's iPLS II software into PDS files for use with PLDasm software.

Merge, allows you to combine multiple PDS files into a single Intel PLD or FPGA.

Change Directory, List Directory, or **Invoke DOS Shell.**

Modify Options to change the text editor, programming software, printer port, hot keys, and other options.

Databook—View datasheet briefs on Intel μPLDs and technical notes on using the software/devices, device order codes, and other pertinent technical information.

PLDasm COMPILATION/SIMULATION

PLDasm software compiles PALASM 2-compatible source files to produce JEDEC files for Intel μPLDs. The typical design process is to create the source file, compile/simulate the design to create a JEDEC file, and program devices. Error, report, and waveform files are viewed throughout the cycle. The edit/compile/simulate/view process is repeated until a design is working as desired. Devices are programmed at the end of the cycle. PLDshell Plus software also offers the ability to edit/simulation/view without "fitting". This allows you to concentrate on logic design first, then fit the working design into a device.

PLDasm software offers the following features:

- Preserves your investment in learning a PLD design language and in developing source files by compiling an industry-standard language.
- Implements designs using Boolean equations, State Machine syntax, or Truth Tables *(Truth Table design is a PLDasm superset feature).*
- Functionally simulates designs.
- Estimates design fit quickly based on basic resource criteria.
- Maps designs into device resources and performs basic logic minimization.
- Generates JEDEC programming files; these files include programming test vectors based on simulation output.

You can compile .PDS files for common PAL/GAL devices using PLDasm software. PAL/GAL designs are transparently converted into JEDEC files for the appropriate Intel μPLD.

DESIGN MERGE

PLDshell Plus can merge multiple PDS design files into any Intel programmable logic device, including the Intel FLEXlogic family of FPGAs. The Merge function makes it easy for designers to consolidate multiple PLDs into a single, high-performance FPGA or PLD.

JEDEC DISASSEMBLY

PLDshell Plus provides the ability to disassemble existing JEDEC files for Intel μPLDs, as well as for common 20-pin and 24-pin PALs and GALs into PLDasm source files. JEDEC disassembly allows you to reconstruct source files for existing designs where the original source files have been lost, or to generate source files from existing designs to be modified for new designs. JEDEC disassembly is available via the **Utilities—Disassemble** menu selections. Note that the source file output during the disassembly process using PAL/GAL JEDEC files is for the respective Intel μPLD.

JEDEC CONVERSION

PLDshell Plus provides the ability to convert existing JEDEC files for common PALs/GALs into JEDEC files for Intel μPLDs. A PLDasm source file is automatically generated during the conversion process. Conversion guarantees that the target Intel μPLD is functionally the same as the original design. JEDEC conversion is available via the **Utilities—Convert** menu selections.

TRANSLATION

PLDshell Plus provides the ability to translate existing ADFs (Advanced Design Files) or SMFs (State Machine Files) into PDS files for use with PLDshell Plus. This provides an automated path for users of Intel's iPLS II software to move to PLDshell Plus and make use of its more powerful simulation features and user interface. Translations is available via the **Utilities—Translate** menu selections.

SYSTEM REQUIREMENTS

PLDshell Plus is designed to work in systems configured as follows:

- Intel 386-based PC with 2 Mbytes of extended RAM
- MS-DOS V3.1 or later
- High-density (1.44 Mbytes) diskette drive; call Intel's EPLD Hot Line or your Intel field sales representative for other disk formats.
- Hard disk with approximately 5 Mbytes of space (4 Mbytes for installation, up to 1 Mbyte for working files while running).
- VGA monitor required for waveform viewing.

ORDERING INFORMATION

PLDshell Plus software (no programming hardware) is available from Intel Literature or your local Intel salesperson. (Quantity limited per order.)

DSPLUSKIT includes PLDshell Plus software and the iUP-PC programming hardware. Available through Intel-authorized sales offices.